CLAIMS

What is claimed is:

1. An apparatus comprising:

a first amplifier comprising first input terminals and first output terminals, wherein the first amplifier is to amplify an input signal provided to the first input terminals and to provide the amplified input signal to the first output terminals;

a second amplifier comprising second input terminals and second output terminals, wherein the second input terminals are operatively responsive to a second input signal and wherein the second amplifier is to amplify the second input signal and provide the amplified second input signal to the second output terminals; and

a coupling device to provide operative responsiveness by the second input terminals to the first output terminals, wherein a common mode voltage at the first output terminals and the second input terminals are approximately equal.

2. The apparatus of Claim 1, wherein the coupling device comprises a high frequency signal path and a low frequency signal path

3. The apparatus of Claim 1, wherein the first amplifier comprises a differential amplifier.

4. The apparatus of Claim 1, wherein the second amplifier comprises a differential amplifier.

5. The apparatus of Claim 1, wherein the coupling device comprises:

a transistor device comprising first, second, and third terminals;

a resistive element operatively responsive to the second terminal and wherein the second terminal is operatively responsive to at least one of the first output terminals;

a capacitive element operatively responsive to the third terminal and wherein at least one of the second input terminals is operatively responsive to the resistive element and the capacitive element; and

a current source operatively responsive to the capacitive element and the third terminal.

6. The apparatus of Claim 1, wherein the coupling device comprises two coupling devices to couple the first output terminals and second input terminals, and wherein each coupling device comprises:

a transistor device comprising first, second, and third terminals;

a resistive element operatively responsive to the second terminal and wherein the second terminal is operatively responsive to one of the first output terminals;

a capacitive element operatively responsive to the third terminal and wherein one of the second input terminals is operatively responsive to the resistive element and the capacitive element; and

a current source operatively responsive to the capacitive element and the third terminal.

7. The apparatus of Claim 1, wherein a common mode voltage at the first input terminals and the first output terminals is approximately equal.

8. A system comprising:

an amplifier comprising:

a first amplifier comprising first input terminals and first output terminals, wherein the first amplifier is to amplify an input signal provided to the first input terminals and to provide the amplified input signal to the first output terminals,

a second amplifier comprising second input terminals and second output terminals, wherein the second input terminals are operatively responsive to a second input signal and wherein the second amplifier is to amplify the second input signal and provide the amplified second input signal to the second output terminals, and

a coupling device to provide operative responsiveness by the second input terminals to the first output terminals, wherein a common

mode voltage at the first output terminals and the second input terminals are approximately equal;

a retimer system to provide samples of an output signal provided by the amplifier;

a bus to exchange signals with the retimer system.

9. The system of Claim 8, further comprising a memory device operatively responsive to the bus.

10. The system of Claim 8, further comprising a data processor to receive samples from the retimer system.

11. The system of Claim 10, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

12. The system of Claim 10, wherein the data processor is to perform optical transport network de-framing in compliance with ITU-T G.709.

13. The system of Claim 10, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.

14. The system of Claim 10, further comprising an interface to provide and receive signals from the data processor.

15. The system of Claim 14, wherein the interface is compatible with XAUI.

16. The system of Claim 14, wherein the interface is compatible with IEEE 1394.

17. The system of Claim 14, wherein the interface is compatible with PCI.

18. The system of Claim 14, further comprising a switch fabric operatively responsive to the interface.

19. The system of Claim 14, further comprising a packet processor operatively responsive to the interface.